IBIS & VERSALEA

2D / 3D solder bump inspection and metrology systems from Lloyd Doyle
**IBIS & VERSALEA** are interferometer based metrology systems used to look at solder bumps at the silicon/substrate interface.

**IBIS & VERSALEA** can be used for either the die-attach side of the silicon chip or the bumped wafer.

**IBIS & VERSALEA** are extremely accurate and fast instruments which provide information on bump position, bump height and coplanarity.

**IBIS & VERSALEA** are suitable for bumps in the range of 20 - 120μ diameter.

Reflowed solder bumps on electroless nickel-gold
IBIS ......so far

Automated production scale system using JEDEC tray feed

Manual development scale system with full analysis tools for bump metrology
VERSALEA is demonstrated here scanning substrates

The substrates have approx. 3000 bumps per piece

24 pieces scanned and reported in <60 seconds

Accuracy better than 1.0µ at 3σ level
Solder bumping is the accepted method of connecting an IC to its carrier for subsequent mounting to a PCB – so called ‘flip chip bumping’ or ‘direct chip attach’.

Over the next decade, this method will become accepted to mount either the silicon directly to the PCB or as a complete replacement for wire bonded ICs.

Solder bumps are there to provide:

- electrical connection
- thermal conductor for device
- mechanical support and insulation for device

Both 2D and 3D inspection requirements are addressed.
Typical flip chip construction

![Diagram of typical flip chip construction]

- Connection from silicon to substrate
- Connection from substrate to PCB

Typical bump size is 100µ on 200µ pitch with height ranging from 50µ to 100µ over an area of 20mm x 20mm
2D / 3D solder bump inspection

Interferometer schematic

- Light source
- Prism
- CCD camera
- Oscillating mirror
- Measured object
- Z axis height measurement
2D / 3D solder bump inspection

- Typical bump inspection machine
  - Stand alone option
  - Full line integration options

- Optical head components
- Samples mounted in isolated holders
- Automatic loading and unloading
2D / 3D solder bump inspection

Typical result after scanning bump area on substrate

This schematic representation shows bump field with colours representing bump heights and gives an immediate feel for solder bump formation process.
2D / 3D solder bump inspection

SEM of coined bump

Height measurement for coined bump sample
2D / 3D solder bump inspection

Greyscale image of sample area

Corresponding digital image of same 
area showing defects

Greyscale and digital comparisons
**Chip carrier system specification:**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>Maximum sample size</td>
<td>50mm x 50mm</td>
</tr>
<tr>
<td>Maximum scan size (single scan)</td>
<td>15mm x 20mm</td>
</tr>
<tr>
<td>Extended scan area (multi scan)</td>
<td>28mm x 38mm</td>
</tr>
<tr>
<td>Maximum ‘out of plane’ distance permissible</td>
<td>≤100µ</td>
</tr>
<tr>
<td>Scan time for good substantially flat specimen</td>
<td>approx 0.5 secs</td>
</tr>
<tr>
<td>Resolution (3D)</td>
<td>0.05µ</td>
</tr>
<tr>
<td>Pixel size (2D)</td>
<td>8.75µ</td>
</tr>
<tr>
<td>Repeatability at 3σ level</td>
<td>better than 1.0µ</td>
</tr>
</tbody>
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- Bump inspection opens up a new range of opportunities
- Up to 3000 devices per hour capacity
- Future developments
  - Die bumps
  - Wafer bumps
  - BGA bumps